Q_{12}, Q_{11}' and Q_{12}', ..., Q_{n-2} and Q_{n-1}, and Q_{n-2}' and Q_{n-1}' having source areas that are commonly connected except for connection control transistors Q_{10}, Q_{10}', Q_n and Q_n' adjacent to the sense amplifiers 110a and 110b. The structures of other parts are the same as those of the schematic circuit diagram shown in FIG. 2.

Please replace the paragraph beginning at page 11, lines 20 -25 with the followings:

FIG. 6 shows a diagram of the layout of the isolation area 129 shown in FIG. 5, and FIGS. 7A through 7C show cross sections taken along lines III-III, IV-IV, and V-V, respectively, of FIG. 6. Local bit lines 108a and 109a which extend in the x-direction are disposed in cell array blocks CAB_{12} and CAB_{13}. Interlayer insulating layers 110, 116, and 120, shown in FIGS. 7A through 7C, are disposed between the local bit lines 108a and 109a and global bit lines 124, 125, and 126 that extend in the x-direction.

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Please replace the paragraph beginning at page 11, line 26 and ending on page 12 line, 5 with the following:

An active area 142 and gate electrodes 143a and 143b for forming select control transistors Q_{15} and Q_{16} included in the isolation area 129 of FIG. 5 are disposed between the cell array blocks CAB12 and CAB13. The gate electrodes 143a and 143b include gate oxide layers 91, polysilicon layers 92, and refractory metal silicide layers 93, as shown in FIGS. 7A and 7B. Silicon nitride layers 94 and spacers 95 on the refractory metal silicide layers 93 are not shown in FIG. 6. The gate electrodes 143a and 143b extend in the y-direction. The local bit line 108a in the first row and the local bit line 108a in the third row are connected to global bit lines 124 and 126, respectively, via plugs 106c and 106d filling contact holes C_{11} and connectors 108b extending from the local bit lines 108a. The active area 142 between the gate electrodes 143a and 143b is connected to the global bit line 124 via plugs 106g and 118a of FIGS. 7A and 7C and the pad 122a, as shown in FIG. 7C. The active area 142 between the gate electrodes 143a and 143b is also connected to the global bit line 126 via plugs 106h and 118b along with the pad 122b, as shown in FIG. 7C. Thus, contact holes C_{11}, C_{12}, and C_{13}, shown in FIG. 7C are filled.

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Please replace the paragraph beginning at page 12, line 6-16 with the following:

A connection between the local bit line 109a in the second row disposed in the two cell array blocks CAB_{12} and CAB_{13} and the global bit line 125 is not shown in FIGS. 6 and 7A through 7C. A dummy local bit line 109b formed on dummy gate electrodes DG_4 and

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DG_5 is connected to the global bit line 125 via dummy plugs 119a and 119b filling contact holes C_{12} and dummy pads 123a and 123b. The spacing between the global bit line 124 disposed in the active area 142 of the isolation area 129 and the adjacent global bit line 125 is d_2. Local bit line connectors 108b are disposed in the first and third rows in the isolation area, 129 and the pitch of the local bit line connector 108b is twice the pitch of the global bit line. Thus, in this case, the margin of a process for forming the contact holes C_{12} and C_{13} is increased compare to the case where the pitch of the local bit line connectors 108b is equal to the pitch of the global bit lines 124, 125, and 126.

Please replace the paragraph beginning at page 12, line 17, and ending on page 13 line, 5 with the following:

With reference to FIGS. 7A through 7C, isolation layers 102 for isolating the cell array block CAB_{12} and the cell array block CAB_{13} from the isolation area 129 are formed on a semiconductor substrate 100. The cell array blocks CAB_{12} and CAB_{13} include gate electrode structures CG_4, CG_5, CG_6, CG_7, CG_8, CG_9, CG_{10}, CG_{11}, CG_{12}, CG_{13}, CG_{14}, and CG_{15} of cell transistors, each having gate oxide layers 91, polysilicon layers 92, refractory metal silicide layers 93, silicon nitride layers 94, and nitride spacers 95. Dummy gate electrode structures DG_2, DG_3, DG_4, DG_5, DG_6, and DG_7 are formed on the isolation layers 102, and connection control transistors $Q_{15}$and Q_{16} are formed in the isolation area 129 of FIG. 6. Local bit lines 108a are formed on first interlayer insulating layers 104 in the cell array areas, and connectors 108b are formed as extensions of the local bit lines 108a. The local bit lines 108a are connected to the semiconductor substrate 100, more particularly, to the active areas 142 of the cell transistors via plugs 106a and 106f. The local bit line connectors 108b for connecting the local bit lines 108a to the connection control transistors Q_{15} and Q_{16} are connected in common to source areas of the connection control transistors Q_{15} and Q_{16} via plugs 106c and 106d. The connectors 108b are also connected to the dummy gate electrode structures DG_2 and DG_3. Capacitors 114a, 114b, 115a, and 115b are formed in the cell array areas on second interlayer insulating layers 110 which cover the local bit lines 108a, 109a, and 109c. The capacitors 114a, 114b, 115a, and 115b are connected to cell transistors via plugs 112a, 112b, 113a, and 113b formed in the first and second interlayer insulating layers 104 and 110. A third interlayer insulating layer 116 covers the capacitors 114a, 114b, 115a, and 115b. Global bit lines 124, 125, and 126 are formed a fourth interlayer insulating layer 120 overlying the third interlayer insulating layer 116.